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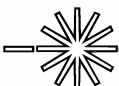
## Vocoder Development Support Tool (VDST)

### Unit Manual



**This document has been prepared for:**

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## 1.0 INTRODUCTION

This Unit Manual provides detailed information about the Vocoder Development Support Tool (VDST).

The VDST has been developed for the **NEXCOM Group (ACB-560)** of the Federal Aviation Administration's William J. Hughes Technical Center. The NEXCOM Group supports the following NEXCOM programs:

- Next Generation A/G Communications System (NEXCOM)
- Rapid Prototype Development Effort (RPDE)
- NEXCOM System Demonstrations

The VDST performs voice encoding/decoding using the NEXCOM standard ATC-10B vocoder algorithm. The VDST supports easy integration with other NEXCOM equipment with both linear and compressed digital voice available on a single multi-slot synchronous serial interface (PCM). Unlike the COTS hardware available from DVSI, the VDST supports truncated mode (compressed voice rate at 4000 bps vice the normal 4800 bps).

### 1.1 PURPOSE

The purpose of this document is to present Vocoder Development Support Tool (VDST) specifications and operating instructions.

The VDST and associated documentation are intended solely to facilitate development of NEXCOM avionics. The VDST and associated documentation neither implies nor imposes functional, performance, design or other requirements, nor in any way alters the existing industry agreements.

### 1.2 DOCUMENT CONVENTIONS

N/A.

### 1.3 INTENDED AUDIENCE AND READING SUGGESTIONS

This document is intended for NEXCOM contractors.

### 1.4 REFERENCES

Reference documentation includes:

- Analog Devices, 218x DSP Hardware Reference, Analog Devices Part Number 82-002010-01.

### 1.5 REVISION HISTORY

| Date       | Revision | Description of Changes  |
|------------|----------|---|
| 07/12/2002 | 1.0      | Initial Release   |
| 11/07/2002 | 2.0      | Incorporated HOST Port Capture and Playback feature documentation. (software release 4.0) |

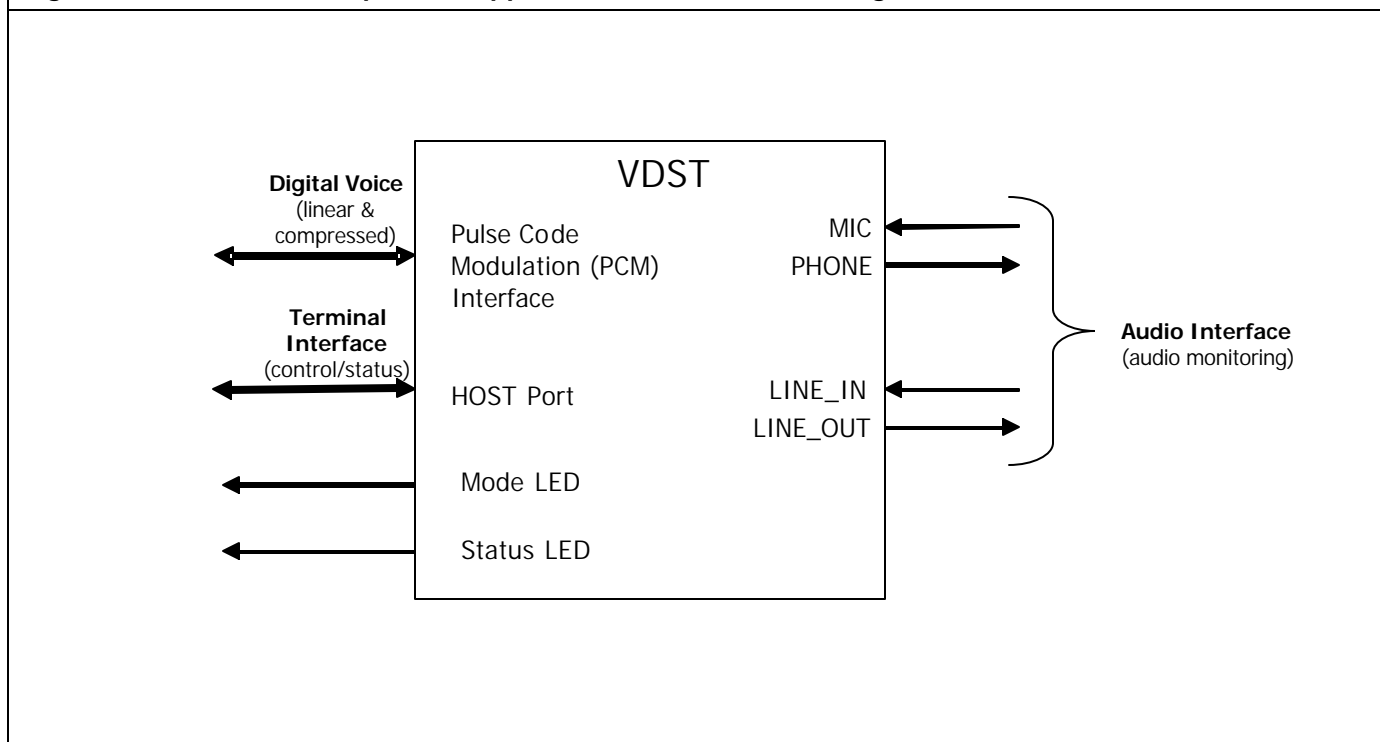


## 2.0 GENERAL DESCRIPTION

### 2.1 OVERVIEW

Figure 1 provides an interface diagram for the Vocoder Development Support Tool (VDST).

**Figure 1. Vocoder Development Support Tool (VDST) Block Diagram**



### 2.2 FEATURES

The Vocoder Development Support Tool (VDST) provides the following features:

- Normal and Truncated Compression Modes (on-the-fly transition)
- Internal/External Clocking
- Full Duplex Audio Monitoring (at headset jacks or at line interface)
- Test Loopback Capabilities at Audio and PCM ports
- Transmit/Receive Compressed Voice Packet FIFO buffers (supports one full TDMA MAC cycle of voice)
- Silence Packet Generator
- Power On Self Test (POST)
- Host Port Capture/Playback of Compressed Voice Messages



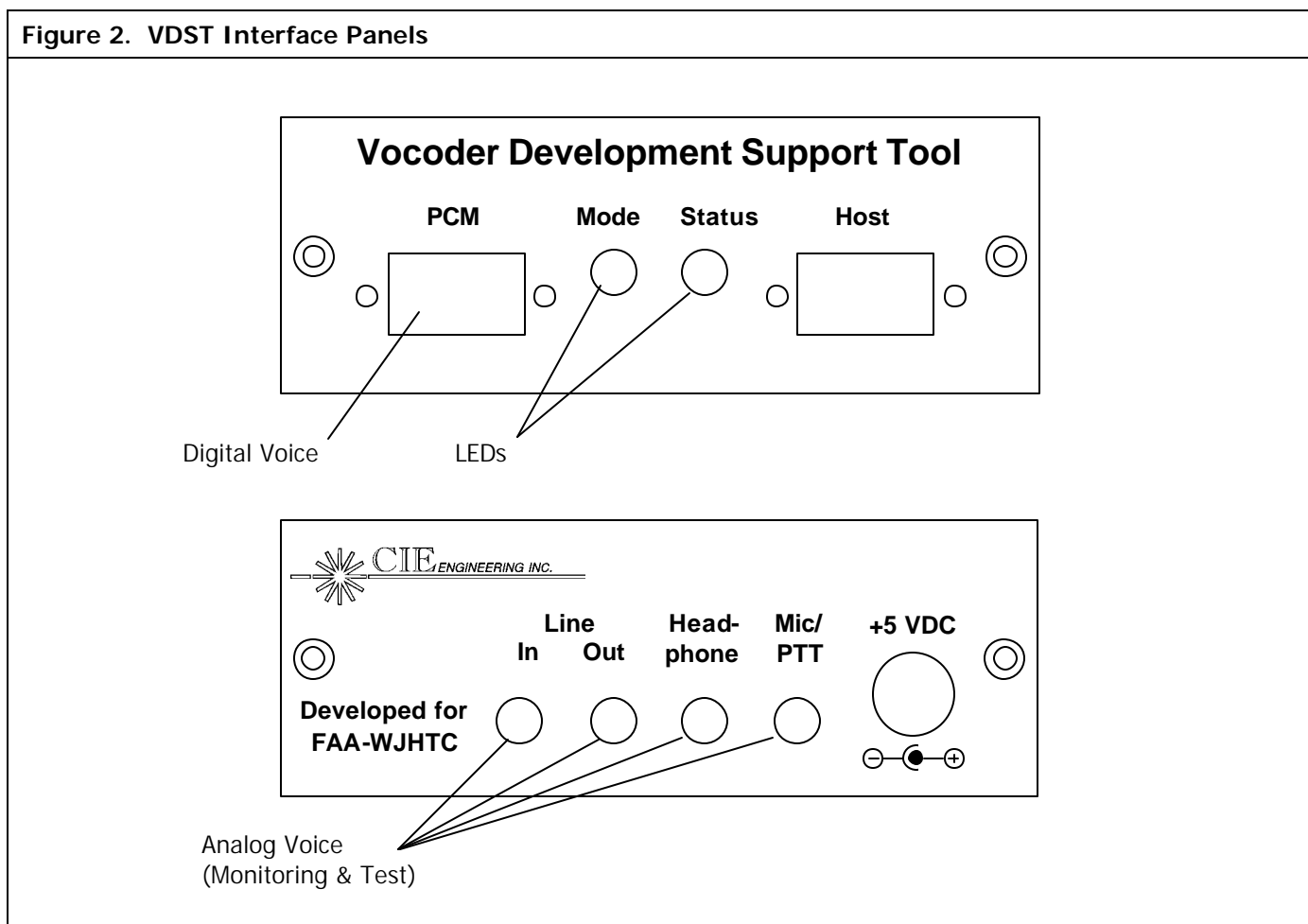
### 3.0 CONNECTORS & INDICATORS

The VDST includes the following connectors and LED displays:

- PCM Interface (1 each) – primary digital interface for linear/compressed voice
- HOST Interface (1 each) – terminal command interface for unit configuration
- Audio Interfaces (4 each) – analog audio for monitoring and test
- Power Interface (1 each) - compatible external DC power supply (supplied with VDST)
- LED Indicators (2 each) –unit mode and status information

Figure 2 contains illustrations of the VDST interface panels showing the location of connectors and LEDs. The following sections contain connector/pinout and LED display information. See "4.0 UNIT OPERATION" for functional information.

**Figure 2. VDST Interface Panels**



### 3.1 PULSE CODE MODULATION (PCM) INTERFACE

The Pulse Code Modulation (PCM) interface provides the primary interface for linear and compressed digital voice communication. The data is transmitted serially using a time division multiplex (TDM) data stream. Standard +3.3 V HCMOS (+5 V tolerant) logic is used. Table 1 provides connector pin and signal information.

| Table 1. Pulse Code Modulation (PCM) – Signal Descriptions (J8) |               |          |   |
|---|---------------|----------|---|
| Symbol  | Pin           | Pin Type | Name/Function   |
| PCM_CLK   | 5             | I/O      | <p><u>PCM Bit Clock</u>: Synchronous clock used for PCM_TD and PCM_RD bit transfer. This clock is an input in EXTERNAL timing mode and an output when the VDST is configured for INTERNAL timing mode.</p> <p>EXTERNAL mode clock rates between 580 kHz and 6 MHz are supported. The standard INTERNAL mode clock rate is 4.096 MHz (other internal clock rates are also available)</p> |
| PCM_TD  | 4             | I/O      | <u>PCM Transmit Data</u> : This pin is configured as an output in DTE communication mode and an input in DCE MODE.  |
| PCM_RD  | 3             | I/O      | <u>PCM Receive Data</u> : This pin is configured as an input in DTE mode and an output in DCE mode.   |
| PCM_FS  | 2             | I/O      | <u>PCM Frame Sync</u> : This pin marks the beginning of a TDM frame of data. This signal is an input in EXTERNAL timing mode and an output when the VDST is configured for INTERNAL timing mode.  |
| GND   | 1, 6, 7, 8, 9 | GND      | <u>Signal Ground</u>  |

The VDST PCM\_CLK and PCM\_FS signal directions are determined by the timing mode (INTERNAL or EXTERNAL). The VDST PCM\_TD and PCM\_RD signal directions are determined by the data mode (DCE or DTE). When switching timing mode, the user must enter HOST port reconfiguration command AND reconfigure internal switches. When switching data mode, the user must reconfigure internal switches ONLY (no HOST port command is required). See "4.3.3 Timing Modes (INTERNAL/EXTERNAL)" and "4.3.4 Data Modes (DTE/DCE)" for more information.

The VDST PCM connector is a standard DB-9M (male pins).





### 3.2 HOST INTERFACE

The Host Interface is used to set VDST configuration parameters. It is compatible with standard computer RS-232 serial ports. The VDST HOST interface is permanently configured as a DCE device. A standard one-to-one interface cable can be used for PC-to-VDST communication. A terminal emulation program, e.g. HyperTerminal, can be used to communicate with the VDST HOST interface.

**Table 2. Host Interface (HOST) – Signal Descriptions (J5)**

| Symbol   | Pin | Pin Type | Name/Function                     |
|----------|-----|----------|-----------------------------------|
| HOST_CD  | 1   | O        | <u>Carrier Detect</u> : Not used. |
| HOST_RD  | 2   | O        | <u>Receive Data</u> :             |
| HOST_TD  | 3   | I        | <u>Transmit Data</u> :            |
| HOST_DTR | 4   | I        | <u>Data Terminal Ready</u> :      |
| GND      | 5   | GND      | <u>Signal Ground</u>              |
| HOST_DSR | 6   | O        | <u>Data Send Ready</u> :          |
| HOST_RTS | 7   | I        | <u>Request to Send</u> :          |
| HOST_CTS | 8   | O        | <u>Clear to Send</u> :            |
| HOST_RI  | 9   | O        | <u>Ring Indicator</u> : Not used. |

*Note: VDST Software Release 4.0 uses hardware flow control (default) to support HOST port Capture and Playback capabilities.*

The VDST HOST connector is a standard DB-9F (socket type pins). The HOST interface uses the standard asynchronous ASCII communication protocol with the following communication parameters:

- 115200 bps, 8 data bits, 1 stop bit, no parity, hardware flow control.

VDST configuration parameters are stored in 'soft' configuration registers' or CREGs. To modify the configuration, a user enters the CREG address and a new value at the terminal interface. See "5.0 CONFIGURATION REGISTERS" for more information.



### 3.3 AUDIO INTERFACES

The VDST includes headset and line interface jacks. The headset interface supports a microphone input, a balanced headphone output and a push-to-talk (PTT) signal. The line interface is compatible with standard 600  $\Omega$  audio interfaces (see note at bottom of the page). See Table 3 through Table 6 for tip, ring, and sleeve signal information.

**Table 3. Microphone/PTT Interface (MIC/PTT) – Signal Descriptions (J17)**

| Symbol | Pin  | Pin Type | Name/Function               |
|--------|------|----------|-----------------------------|
| MIC    | TIP  | I        | Microphone Input:           |
| PTT    | RING | I        | Push to Talk (PTT) Control: |
| GND    | SLV  | GND      | Signal Ground               |

**Table 4. Headphone (HEADPHONE) – Signal Descriptions (J16)**

| Symbol | Pin  | Pin Type | Name/Function            |
|--------|------|----------|--------------------------|
| PH+    | TIP  | O        | Headphone Output (TIP):  |
| PH-    | RING | O        | Headphone Output (RING): |
| NC     | SLV  | NC       | No connection.           |

**Table 5. Line Input (IN) – Signal Descriptions (J14)**

| Symbol | Pin  | Pin Type | Name/Function      |
|--------|------|----------|--------------------|
| IN+    | TIP  | I        | Line Input (TIP):  |
| IN-    | RING | I        | Line Input (RING): |
| NC     | SLV  | NC       | No connection.     |

**Table 6. Line Output (OUT) – Signal Descriptions (J15)**

| Symbol | Pin  | Pin Type | Name/Function       |
|--------|------|----------|---------------------|
| OUT+   | TIP  | O        | Line Output (TIP):  |
| OUT -  | RING | O        | Line Output (RING): |
| NC     | SLV  | NC       | No connection.      |

*Note: The interfaces will function with standard computer audio equipment, e.g. computer sound card; however, care must be used in connecting the interfaces. Computer interfaces are designed for unbalanced, stereo interfaces (left audio on tip, right audio on ring, and a grounded sleeve). The VDST requires a balanced interface signal. Construct an adapter cable, as required.*



### 3.4 POWER INTERFACE

The VDST requires an external power supply which provides a regulated +5 VDC power rail (@ 1.5 A max). The power jack is a standard 2.1 mm power connector (tip=+5 V, ring=GND). The VDST is supplied with a compatible external power supply.

### 3.5 LED INDICATORS

The VDST provides two LED indicators. Although the LEDs are bicolor (RED/GREEN), the VDST uses a fast RED/GREEN toggle to create a third state, i.e. YELLOW. Table 7 describes the three states for each LED.

| Table 7. LED Indicators |              |   |   |
|-------------------------|--------------|---|---|
| LED Indicator           | GREEN        | YELLOW  | RED   |
| MODE                    | Normal Audio | Truncated Audio   | Blinks RED when peak audio is detected.   |
| STATUS                  | Okay         | ER bit on PCM interface is set.<br><br>See CREG 0x001C for source of error. | Loss of signal on PCM interface or frame sync for PCM interface being received at incorrect rate. |

*Note: If both the status and the mode LED are simultaneously blinking RED, the VDST has failed power on self test.*

*Note: The 'YELLOW' indication is created by a fast GREEN/RED toggle. Viewing angle may affect viewed color.*



## 4.0 UNIT OPERATION

This section covers the following areas:

- Operation Modes – provides general information about normal and truncated modes
- Voice Functional Flow – presents voice flow/routing information
- PCM Operation – provides frame format and bit assignment information
- Compressed Voice Transfer – presents sequencing for transferring compressed voice packets

### 4.1 OPERATIONAL MODES (NORMAL/TRUNCATED)

The VDST supports three operational modes:

- Normal Mode: (OPMODE = 1) The PCM frame rate is 8000 frames/second (fps) and analog audio sample rate is 8000 samples/second (sps). The vocoder is compressing audio at a normal rate.
- Truncated 8000 Mode: (OPMODE = 2) The PCM frame rate is 8000 fps. The analog audio sample rate is 6667 sps. The vocoder operates on 24 millisecond vocoder frame boundaries. This mode includes a rate adaptation module to convert 8000 sps linear audio to 6667 sps linear audio.
- Truncated 6667 Mode: (OPMODE = 3) The PCM frame rate is approximately 6667 fps (the exact frame rate is  $5/6 \times 8000$  fps). The analog audio sample rate is 6667 sps. The vocoder operates on 24 millisecond vocoder frame boundaries. Rate adaptation is NOT required.

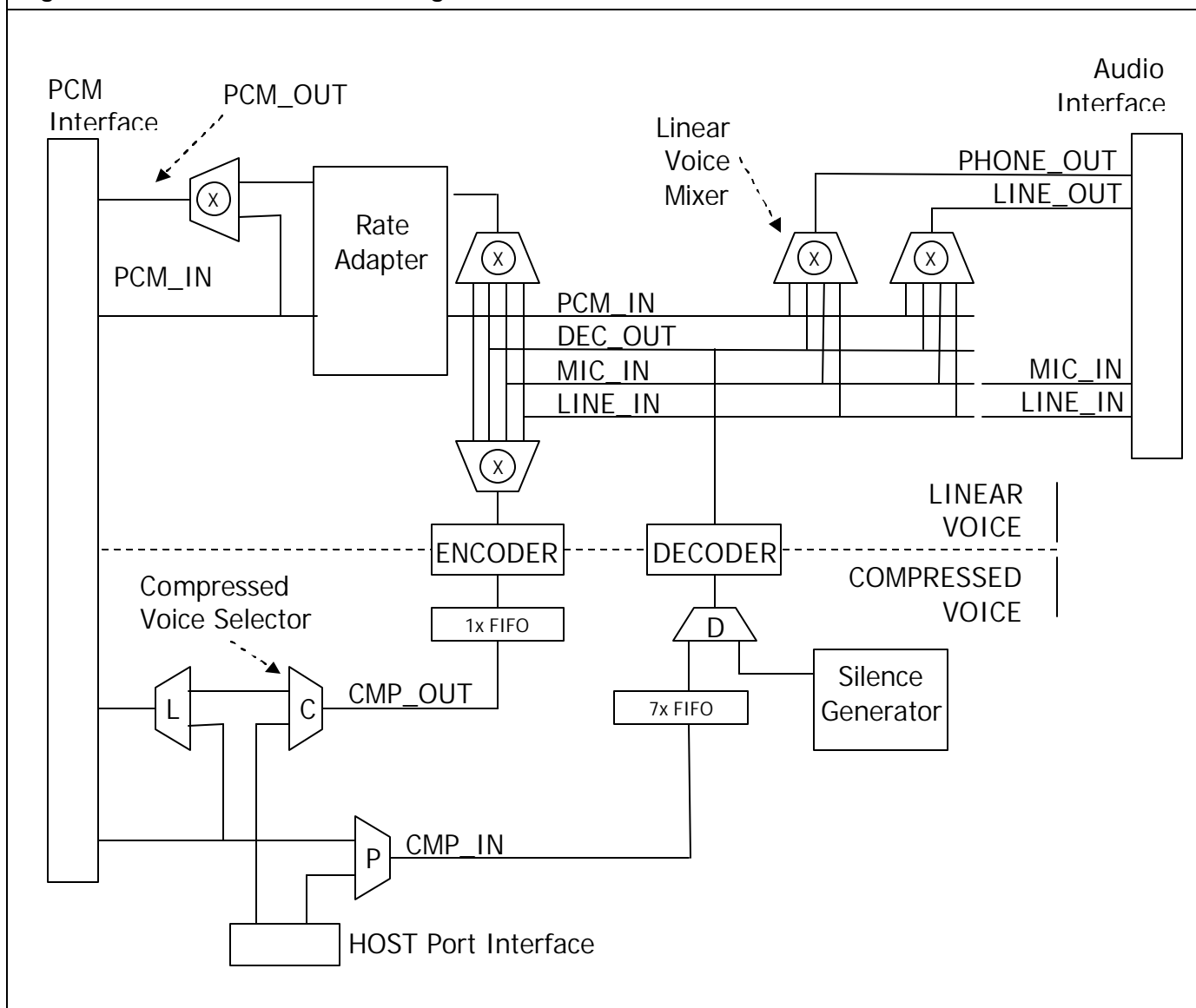
Since the truncation mode type (8000 or 6667 fps) is configured at the HOST interface, a typical system only uses one truncated mode type. The mode type is saved in non-volatile memory and is retained after power cycling.

The truncated modes result in a lower compressed voice bit rate, i.e. 4000 bps versus 4800 bps. The VDST supports on the fly transition between normal and truncated modes. The on-the-fly transition is controlled by the TM bit in the Control/Status word via the PCM interface.

## 4.2 VOICE FUNCTIONAL FLOW

Figure 3 provides a functional voice flow diagram. The figure is divided into two major sections: linear voice and compressed voice. The linear voice section contains four linear voice mixers with input volume control. The compressed voice section contains four compressed voice flow selectors (i.e., switches). The DVSI vocoder (encoder and decoder) are located at the boundary between the linear and compressed voice regions of the diagram.

**Figure 3. Functional Voice Flow Diagram**



The PCM interface carries both linear (PCM\_IN/PCM\_OUT) and compressed (CMP\_IN/CMP\_OUT) digital voice. Linear voice is placed in timeslot 0 and compressed voice is sent as a packet/message in the system field within timeslot 1. Detailed PCM interface information can be found in "4.3 PCM Operation". Detailed information about HOST port interface compressed voice 'capture' and 'playback' information can be found in "4.5 Compressed Voice Transfer (HOST Port)".

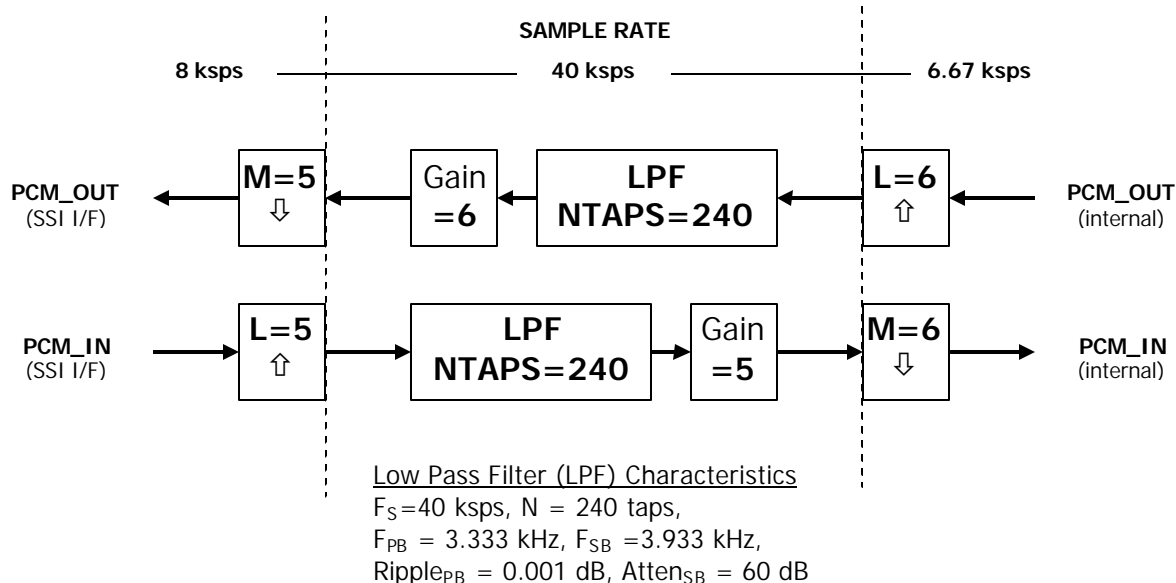


The subsequent sections present information on the major functions including the Rate Adapter, Linear Voice Mixer, Compressed Voice Selector, Compressed Voice FIFOs, and the Silence Generator.

### 4.2.1 Rate Adapter

The rate adapter uses a multi-rate filter to convert 8 kbps voice to 6.667 kbps voice (required for OPMODE = 2). The rate adapter is 'in place' for the remaining two operational modes, but is configured for 'bypass' operation. Figure 4 contains a block diagram of the rate adapter.

**Figure 4. Rate Adapter Block Diagram**



The rate adapter uses a multi-rate filter with a rational rate change (L/M) of either 6/5 or 5/6, depending on the direction. A zero sample insertion algorithm is used in interpolating the signal to produce a 40 Kbps sample rate. This approach maintains spectral purity, but introduces a 1/L amplitude reduction. A follow-on gain stage compensates for the power reduction.

A computationally efficient low pass filter provides signal smoothing after the interpolator (↑). The polyphase filter implementation reduces the number of computations by eliminating computations associated with the zero-valued samples (inserted by the interpolator). A total of N/L computations per sample are required rather than N computations.

The filter provides a very flat passband response (ripple less than 0.001 dB) with a very sharp cutoff for signals above 3.333 kHz. The signal is attenuated by 60 dB over a transition band of 600 Hz. The cutoff frequency was designed to reduce aliasing at the 6.667 kbps rate, i.e. it is set equal to  $0.5 \cdot F_S$ .

The bypass implementation is implemented by adjusting the decimator (↓) value to match the interpolator value. This provides a rational rate change of  $L/M = 1$  (for  $M=L$ ) and maintains a constant audio delay for both normal and truncated operational modes. A constant audio delay enables a 'one-time' vocoder alignment to minimize system audio delays in either normal or truncated operational modes. The one-way audio delay through the rate adapter is equal to  $0.5 \cdot NTAPS/F_S$  or 3 ms.

### 4.2.2 Linear Voice Mixer

The mixers enable one or more audio signals to be summed (with independent input volume controls) to create an output signal. A mixer is located at each of the four linear voice outputs: PCM\_OUT, ENC\_IN (output from linear region is provided as an input to the encoder), PHONE\_OUT, and LINE\_OUT. By adjusting the volume settings for each of the four signals entering a mixer, the user can effectively 'alter' voice signal flow. For example, the LINE\_OUT signal can be configured to monitor any one or more of the four linear input signals: PCM\_IN, DEC\_OUT, MIC\_IN, or LINE\_IN. Thus, loop backs can be created and full duplex audio monitoring (air-to-ground/ground-to-air) can be implemented.

The default configuration supports a full duplex audio monitoring configuration. The headphone and line output signals monitor the linear voice input and output signals at the PCM interface. The detailed default configuration is provided below:

- $\text{PHONE\_OUT} = (\text{VOL\_PCM\_IN} = 0x7FFF) * \text{PCM\_IN} + (\text{VOL\_DEC\_OUT} = 0x7FFF) * \text{DEC\_OUT}$   
Enables user to monitor both the linear voice input and output signals.
- $\text{LINE\_OUT} = (\text{VOL\_PCM\_IN} = 0x7FFF) * \text{PCM\_IN} + (\text{VOL\_DEC\_OUT} = 0x7FFF) * \text{DEC\_OUT}$   
Enables user to monitor both the linear voice input and output signals.
- $\text{PCM\_OUT} = (\text{VOL\_DEC\_OUT} = 0x7FFF) * \text{DEC\_OUT}$   
Connects the decoder output to the user.
- $\text{ENC\_IN} = (\text{VOL\_PCM\_IN} = 0x7FFF) * \text{PCM\_IN}$   
Connects the encoder input to the user.

To connect an input to the mixer, set the input volume level to 0x7FFF. To disconnect an input, set the input volume level to 0x0000. To adjust the volume level, select a level between 0 and 0x7FFF.

### 4.2.3 Compressed Voice Selector

There are four compressed voice selectors that 'route' voice packets.

The Loop Selector (L) is controlled by a soft configuration register, i.e. CREG[0x1F]. It supports a compressed voice loop-back capability at the PCM interface, i.e. no vocoder in the path. This feature supports the testing of compressed voice packet transfers. The selector is still operational during host port capture and playback.

The Decoder Selector (D) is controlled by the SI silence bit in the PCM bus system data field. The Decoder Selector actually has manual and automatic characteristics. When the user has asserted the SI bit in the stream, the VDST sends the decoder a packet stream that produces silence on the output. This is a 'manual' control. The VDST will also insert packets from the silence generator IF the decoder input queue underflows (runs empty). This is the 'automatic' function of the compressed voice selector.

The Capture Selector (C) is controlled by the Host Port Capture register, i.e. CREG[0x25]. When the capture mode is selected, compressed voice packets are routed from the encoder to the Host Port interface.

The Playback Selector (D) is controlled by the Host Port Playback register, i.e., CREG[0x26]. When the playback mode is selected, compressed voice packets are routed from the Host Port interface to the decoder.

#### 4.2.4 Silence Generator

The silence generator produces a packet stream that results in silence at the linear output of the decoder. The VDST will automatically provide the decoder with silence packets if the decoder input queue underflows (runs empty). The user can force the VDST to insert the silence packet stream via the SI bit (during runtime operation).

#### 4.2.5 Compressed Voice Message Queues (FIFOs)

The VDST includes voice packet queues in the encoder output and the decoder input paths. A voice packet contains 96 bits (or 12 bytes). The information contained in a voice packet generates 20ms of linear audio (after the packet is decoded).

The encoder queue is sized at 1X packet depth. Voice packets have the highest priority for transmission at the PCM interface, thus the 1X size is sufficient. The decoder queue is sized at 7X packet depth. The size supports a full VDL Mode 3 MAC cycle burst, i.e. up to 6 voice packets or 120 ms, plus one packet.

The queues can be flushed using the RB reset buffer bit in the PCM bus system data field, timeslot 1.

#### 4.2.6 PCM Interface Loopback

The VDST also supports an aggregate loopback at the PCM interface. A soft configuration register, i.e. CREG[0x1F], controls the PCM Loopback.

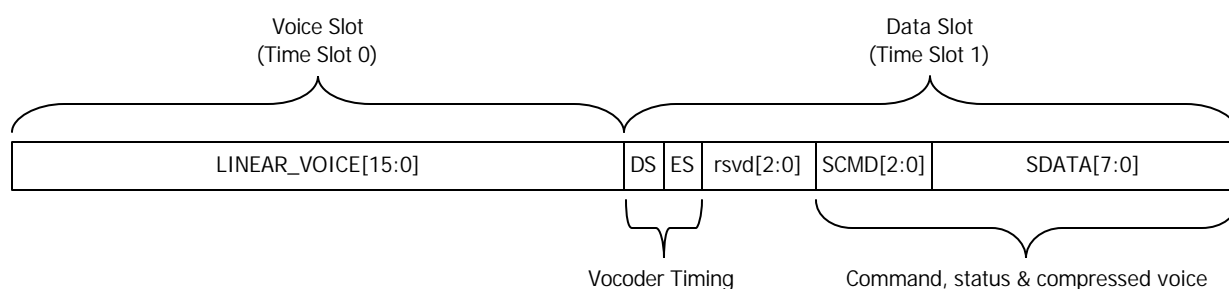


## 4.3 PCM OPERATION

### 4.3.1 Frame Format

The PCM frame format includes two timeslots: a voice slot that carries linear 16-bit voice samples and a data slot. The data slot is divided into two regions: a vocoder timing bit region and a system command/data field. See Figure 5.

**Figure 5. PCM Frame Format**



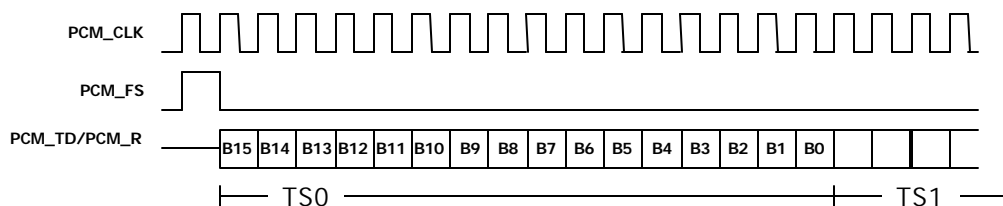
|                     |   |
|---------------------|---|
| <b>LINEAR_VOICE</b> | Linear Voice Data: Linear voice data sent at one 16-bit sample per frame.   |
| <b>DS</b>           | Decoder Sync: A transition from 0 to 1 initiates the start of a new decoder frame.  |
| <b>ES</b>           | Encoder Sync: A transition from 0 to 1 initiates the start of a new encoder frame.  |
| <b>rsvd</b>         | Reserved. Set=0 for future compatibility.   |
| <b>SCMD</b>         | System Command: Defines the contents of the SDATA field.<br>000: Null<br>001: Control/Status Byte<br>010: Compressed Voice Packet (start byte)<br>011: Compressed Voice Packet (next byte)<br>1xx: Reserved |
| <b>SDATA</b>        | System Data: Contains voice, control or status information.   |

The VDST only uses the first two timeslots of the PCM bus. The output data interface (i.e., PCM\_TD in DTE mode) is always active, i.e., the drivers are NOT tri-stated and remain active for all timeslots. The VDST ignores any input data that may be present in other timeslots.

### 4.3.2 Timing Diagram

The VDST uses a time division multiplexed (TDM) bit stream to transfer digital voice and control/status information. The PCM\_CLK provides bit timing and the PCM\_FS signal marks frame boundaries. See Figure 6.

**Figure 6. PCM Timing Diagram**



- PCM\_FS** PCM Frame Sync: The VDST samples the frame sync on the falling edge of the clock. Data bit transfer begins with the next rising edge of the clock. In EXTERNAL timing mode, the VDST samples the PCM\_FS bit on the falling edge of the PCM\_CLK. In INTERNAL timing mode, the VDST outputs the FS bit on the rising edge of the PCM\_CLK.
- PCM\_TD** PCM Transmit Data: In DTE data mode, the VDST outputs bits on the rising edge of PCM\_CLK. In DCE data mode, the VDST samples input bits on the falling edge of PCM\_CLK. Data is transmitted MSB first.
- PCM\_RD** PCM Receive Data: In DTE data mode, the VDST samples input bits on the falling edge of PCM\_CLK. In DCE data mode, the VDST outputs bits on the rising edge of PCM\_CLK. Data is transmitted MSB first.
- PCM\_CLK** PCM Clock: Used for data bit transfer timing.

*Note: The PCM interface is driven by an internal Analog Devices ADSP-2188M serial port interface, i.e. SPORT 0, via a SN74LVCR2245A buffer. Refer to the ADSP-2188M data sheet for detailed timing information, e.g., setup and hold times. The ADSP-2188M oscillator frequency is 36.864 MHz.*



### 4.3.3 Timing Modes (INTERNAL/EXTERNAL)

The VDST supports two types of timing modes: INTERNAL timing mode and EXTERNAL timing mode. In INTERNAL timing mode, the VDST generates PCM\_CLK and PCM\_FS. The default INTERNAL PCM\_CLK and PCM\_FS rates are 4.096 MHz and 8000 fps, respectively. These rates can be reconfigured via the HOST port interface.

To configure the VDST timing mode:

1. Using the HOST port, set CREG[0x17] = 0x0000 to select EXTERNAL timing mode OR CREG[0x17]=0x0001 for INTERNAL timing mode.
2. Using the HOST port, optionally reconfigure the PCM\_CLK and PCM\_FS rates using CREG[0x18] and CREG[0x19]. Refer to the ADSP-2188M SCLKDIV and RFSDIV registers, respectively, noting that the DSP oscillator frequency is set at 36.864 MHz. This step is ONLY required for INTERNAL timing mode.

*Note: The internally generated PCM\_CLK frequencies available are provided by the following equation:  $PCM\_CLKfreq = 36864000/(SCLKDIV+1)$  where  $SCLKDIV = \{5...63\}$*

3. Use the HOST port to SAVE (CREG[0x12]=0xab10) the new settings to non-volatile memory.
4. Remove VDST power and open up the VDST case. Slide out the printed circuit board (PCB) assemblies. Remove the DVSI vocoder from the top of the VDST base board.
5. Locate switch bank, SWA, and configure the switches as shown in Table 8. The switch, SWA, is located right next to the PCM DB-9 connector.
6. Reassemble the vocoder/VDST PCB assemblies and slide them back into the case. Close the case. Apply power. The VDST must be power cycled to recognize the new serial port settings. These settings are checked only during boot-up operation.

**Table 8. INTERNAL/EXTERNAL Timing Mode Switch Settings (SWA)**

| #1  | #2  | #3 | #4 | #5 | #6 | #7  | #8  | Timing Mode          |
|-----|-----|----|----|----|----|-----|-----|----------------------|
| OFF | ON  | X  | X  | X  | X  | OFF | ON  | INTERNAL Timing Mode |
| ON  | OFF | X  | X  | X  | X  | ON  | OFF | EXTERNAL Timing Mode |



#### 4.3.4 Data Modes (DTE/DCE)

The VDST can be configured as a DTE or DCE device for data transmission. Normally, the VDST is configured as a DTE device, thus, PCM\_TD is an output and PCM\_RD is an input.

The PCM data mode can be reconfigured by setting the DCE/DTE Switch Settings on switch SWA. To gain access to the switches, the VDST must be disassembled. Refer to the disassembly instructions in "4.3.3 Timing Modes (INTERNAL/EXTERNAL)". Unlike the timing mode reconfiguration, the data mode configuration does not require any changes to CREGs.

| Table 9. DTE/DCE Data Mode Switch Settings (SWA) |    |     |     |     |     |    |    |  |
|--|----|-----|-----|-----|-----|----|----|--|
| #1   | #2 | #3  | #4  | #5  | #6  | #7 | #8 | Timing Mode  |
| X  | X  | ON  | OFF | OFF | ON  | X  | X  | DTE Data Mode<br>(PCM_TD = output, PCM_RD = input) |
| X  | X  | OFF | ON  | ON  | OFF | X  | X  | DCE Data Mode<br>(PCM_TD = input, PCM_RD = output) |

*Note: Data modes (DTE/DCE) support a planned future capability to support a test configuration that allows one VDST unit to function as a test source for a second VDST unit. In this configuration, the units can be connected with a one-to-one cable with one unit in DCE mode and the second unit in DTE mode.*

#### 4.3.5 Vocoder Timing Bits

The vocoder timing bits are used to set the boundaries (align) the vocoder voice processing window. Proper alignment of the processing window can reduce overall NEXCOM voice delay. The VDST provides the internal vocoder with vocoder frame syncs every 20 milliseconds (or every 24 milliseconds in truncated mode). The external system can force realignment of the processing window by presenting a 0-to-1 transition for the associated vocoder timing bit. Accuracy of alignment is to within 1.1 ms (maximum).

The DS bit is used to align the decoder processing window. The ES bit is used to align the encoder processing window. The alignments of the two windows are independent of one another. Once the alignment is requested, the VDST continues to generate frame syncs at appropriate intervals. Thus, the alignment is typically a one-time event.

*Note: The Compressed Voice Decoder Path packet transfer is initiated with a DS vocoder timing transition (recommended) to insure internal buffers do not underflow. The Compressed Voice Encoder Path packet transfer does NOT require a similar ES vocoder timing bit transition, since underflow is not possible for this path.*

*Note: Audio may become garbled after modification of the ES or DS bits. To clear the garbled audio condition, use either the RB bit on the PCM interface or CREG[0x1d]. Refer to "4.3.6 Control/Status Byte" and "5.4.11 CREG Reset Buffer (0x001D)" for more information.*

*Note: Underflow/overflow errors may be generated immediately after the ES or DS bit has been modified while the system is synchronizing. To clear the error condition use the procedure described in the above note.*



### 4.3.6 Control/Status Byte

The VDST control/status byte is transferred over timeslot 1 of the PCM frame. The control status byte includes the following capabilities:

- User controlled insertion of a silence packet in the decoder path.
- On-the-fly normal/truncation mode control (see TM bit).
- Buffer reset control
- Control byte request (user sets ER bit)
- Control byte response (VDST replies with current bit status)

**Figure 7. Control/Status Byte**



|           |  |
|-----------|--|
| <b>ER</b> | Error: When set in the PCM output stream, it indicates an error. The output error status bit is "sticky", that is, the bit is latched once an error condition is detected. The Reset Buffer Bit can be set to attempt to clear the error. If the error condition was due to a compressed voice packet underflow/overflow condition (or if the error has been subsequently cleared), the ES output bit is cleared (reset). The state of the bit is ignored in the input PCM stream but it should be set to 0 to ensure future compatibility.  |
| <b>RB</b> | Reset Buffer Bit: When set in the PCM input stream, it commands the VDST to reset the compressed voice packet buffers. The decoder input buffer can hold up to 7 packets of voice information (one complete VDL Mode 3 MAC cycle). The encoder output buffer can hold up to 1 packet of voice information. The reset operation deletes the contents of both buffers. The VDST then allows one packet to be stuffed into the input/output queues before re-enabling packet transmission. The VDST echoes this bit state in the PCM output stream. Insure this bit is subsequently reset to prevent a continual reset condition. |
| <b>SI</b> | Silence Bit: When set in the PCM input stream, it commands the VDST to insert a silence packet in the decoder input queue. A silence packet is required when valid compressed voice information is not available (e.g., a missed MAC cycle burst). The VDST echoes this bit state in the PCM output stream.  |
| <b>TM</b> | Truncated Mode Bit: When set, configures the VDST to operate in truncated mode. The type of truncation mode is configured by the VDST serial port. This bit can be set/reset on the fly to transition the VDST between normal and truncated modes. The user controls this bit in the PCM input stream to set the mode. The VDST echoes this bit status on the PCM output stream.   |

*Note: The current status will be sent by default when compressed voice packets are not being transmitted.*

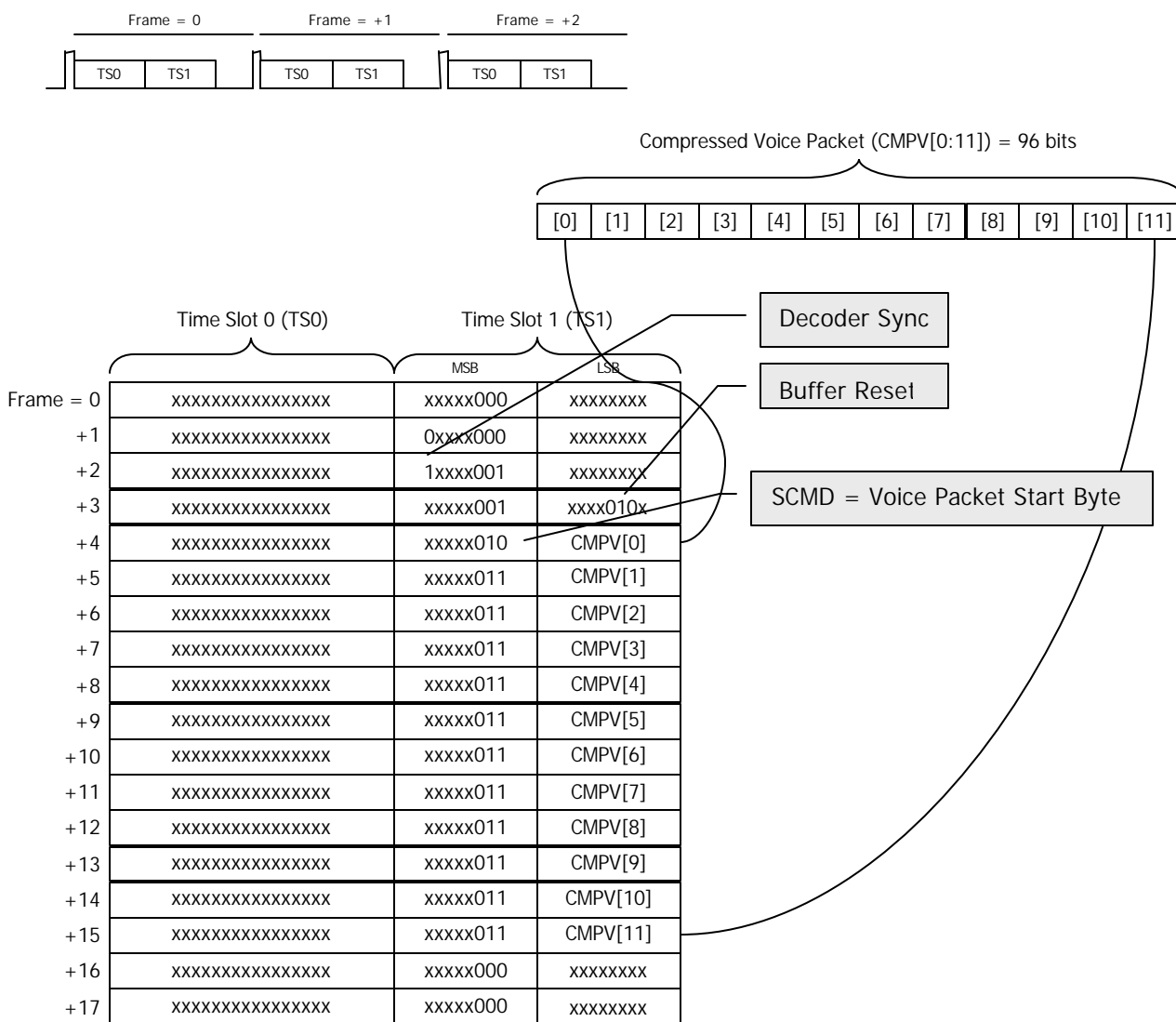


#### 4.4 COMPRESSED VOICE TRANSFER (PCM PORT)

This section describes the transfer of compressed voice packets over the PCM port.

The VDST transfers compressed voice packets via the SCMD and SDATA fields in timeslot 1 of the PCM frame. Each voice packet contains 12 bytes (96 bits). During normal operation, a packet is transmitted every 20 milliseconds (4800 bps). In truncated mode, a packet is transmitted every 24 milliseconds (4000 bps). Figure 8 illustrates the compressed voice packet transfer.

**Figure 8. Compressed Voice Packet Transfer (PCM Port)**



#### 4.4.1 Decoder Path

The VDST supports bursts of up to 7 voice packets in the decoder path, i.e., it buffers up the compressed voice data associated with one complete VDL Mode 3 MAC cycle. In addition, the voice data bytes need not be supplied in a contiguous manner, i.e., other commands can be interleaved within the packet byte stream.

The VDST waits for complete reception of a voice packet before posting the packet to the decoder FIFO queue. Any incomplete packets are discarded. If the decoder FIFO queue is empty (when the next decoder packet must be provided to the vocoder), the VDST will automatically insert a silence packet and set the Error/Status bit (to indicate packet underflow).

The recommended startup sequence for the decoder transmission path is depicted in Figure 8 and listed below:

1. Assert the DS sync input bit (rising edge) to align the vocoder processing window.
2. Reset the buffers.
3. Transfer the first voice packet

The recommended sequence insures that the first voice packet is received by the VDST before it is required and insures an underflow event does not occur on startup. The user must insure the flow of packets is sufficient to prevent decoder buffer underflow/overflow conditions.

#### 4.4.2 Encoder Path

The VDST outputs a compressed voice packet as soon as a complete packet has been received from the vocoder. A packet is transmitted every 20 or 24 milliseconds for normal and truncated modes, respectively.

## 4.5 COMPRESSED VOICE TRANSFER (HOST PORT)

The VDST provides the ability to transfer compressed voice packets via the HOST terminal interface. This enables users to capture and playback voice over a serial port using ASCII text file transfers. The VDST disables processing of PCM timeslot 1 data during capture and playback; thus, the compressed voice packet transfer capability of the PCM port is disabled when either capture or playback is enabled. However, it is critical for the PCM port clocks, i.e., PCM\_CLK and PCM\_FS, to be active and setup up correctly for the system to function properly. In addition, it is important to enable serial port hardware handshaking to control the flow of voice packets over the interface.

This section covers the following areas:

- Host Port Capture (VDST → Host)
- Host Port Playback (Host ← VDST)
- ASCII Compressed Voice Message Format

### 4.5.1 Host Port Capture

The Host Port Capture capability enables the VDST to transmit a stream of compressed voice data over the HOST port. This data can be saved to a file and subsequently played back through the VDST at a later time. When Host Port Capture is enabled, the compressed voice packet transfer capability of the PCM port is disabled. To save the data to a file, it is recommended that the user use a terminal emulation program with file transfer capability.

To capture compressed voice data over the VDST Host serial port:

1. Insure that VDST timing (PCM\_CLK and PCM\_FS) and operational mode are properly configured.
2. Insure the desired linear voice source is applied at the encoder input.
3. Using the HOST port, set CREG[0x25] = 0x0000 to enable the flow of compressed voice data to the HOST port.
4. Enable text capture (file capture) on the terminal emulation program.
5. Capture the desire amount of data.
6. Disable text capture on the terminal emulation program.
7. Press the **ESCAPE** key to stop the transmission of compressed voice data and to exit the Host Port Capture mode.

### 4.5.2 Host Port Playback

The Host Port Playback capability enables the VDST to receive a stream of compressed voice data over the HOST port and to 'play' the decoded audio over the selected linear voice output ports. When Host Port Playback is enabled, the compressed voice packet transfer capability of the PCM port is disabled; however, the user can configure the VDST to transmit the decoded voice over the PCM linear voice timeslot. To playback the data over the HOST port, it is important that the terminal emulation program supports hardware flow control. If hardware flow control is not enabled, the terminal emulation program will overrun the internal VDST buffers. It is also important that the terminal emulation program transmits the compressed audio packets without built-in pauses.



To playback compressed voice data over the VDST Host serial port:

1. Insure that VDST timing (PCM\_CLK and PCM\_FS) and operational mode are properly configured.
2. Insure the linear voice mixers are configured to 'route' the uncompressed audio out the desired port(s).
3. Insure the terminal emulation program is configured to enable hardware flow control
4. Using the HOST port, set CREG[0x26] = 0x0000 to enable the flow of compressed voice data to the HOST port.
5. Transmit the audio text file without any protocol.

*Note: If you are using HyperTerminal and the audio output doesn't sound correct, try enabling the local echo of typed characters just before file transfer. The local echo of typed characters can be disabled again after the file transfer has been complete and before proceeding to the next step. Some versions of HyperTerminal appear to have a software malfunction. Although this program can be supposedly be configured to insure no line pauses are inserted, this feature only seems to function properly when local echo of typed characters is enabled. Alternatively, you may use TeraTermPro (a freeware terminal emulation program distributed on the VDST CD). This program does not have this malfunction and also supports scripting.*

6. Press the **ESCAPE** key to stop the transmission of compressed voice data and to exit the Host Port Playback mode.

During playback, the VDST will print any detected errors to the HOST port. Only a single error message can be generated per packet. If for instance a packet has both a sequence error and a checksum error only a checksum error message will be generated. Error messages consist of a single ASCII character. The error messages are listed by priority (from high to low) in Table 10.

| Table 10. ASCII Compressed Voice Message Errors |   |
|---|---|
| Error Character                                 | Error Condition   |
| L   | Packet is of incorrect length.  |
| 1   | Checksum field contains non-hexadecimal characters.   |
| C   | Calculated checksum does not match checksum field   |
| V   | Incompatible format version.  |
| 2   | Sequence field contains non-hexadecimal characters.   |
| S   | Sequence error. The VDST expects the sequence number to increase by 1 rolling over at 0xffff for every packet transmitted. It is expected that this error message be generated once during startup while the VDST is synchronizing to the new audio sequence. |
| T   | Illegal truncation type   |
| H   | Compressed voice data field contains non-hexadecimal characters.  |



### 4.5.3 ASCII Compressed Voice Message Format

The ASCII Compressed Voice Message Format is defined in Figure 9. The format enables the unit to synchronize at any point and ensures the operational mode is correct (unit will switch to truncated mode when that mode is indicated).

**Figure 9. ASCII Compressed Voice Message Format (HOST Port)**

**VMSSSSXXXXXXXXXXXXXXXXXXXXXXXXXXXXCCCC<cr><lf>**

- V** Format Version: This 1-character field provides the version of the ASCII compressed voice message format. Currently, the VDST only supports message format '0'.
- M** Operational Voice Mode: This 1-character field provides the voice operational mode as follows:
- '0' = OP MODE 1 (Normal Voice Mode)
  - '1' = OP MODE 2 (Truncated Voice – 8KFS)
  - '2' = OP MODE 3 (Truncated Voice – 6KFS)
- SSSS** Line Sequence Number: This 4-character hexadecimal field represents a 16-bit hexadecimal number. It increments by 1 for each line and ranges from 0000 to ffff. The sequence number wraps back to 0000.
- XX...XX** Vocoder Data: This 24-character field contains the 12 byte voice data stream. The left-to-right character sequence corresponds to the proper bit transmission order, i.e. the first bit of the field is transmitted first within the VDL Mode 3 voice bit packet stream.
- CCCC** Checksum: This 4-character hexadecimal field contains a 16-bit checksum computed as follows:
- $$CCCC = \text{hex}(V) + \text{hex}(M) + \text{hex}(S_0) + \text{hex}(S_1) + \text{hex}(S_2) + \text{hex}(S_3) + \\ \text{hex}(X_0) + \text{hex}(X_1) + \dots + \text{hex}(X_{22}) + \text{hex}(X_{23})$$

Example: ...<excerpt from file>

```
000501dea851e1c326ecf0876409f407bc
00050205244d8a6f398c3d7b008b300753
0005035276a651aedc22f3ac1f49c007de
00050477f7a5810a3fd266d3a3ce3e07ea
```

*Note: Text lines are delimited by ASCII 'carriage return' and 'line feed' characters, i.e. <cr> and <lf>.*



## 5.0 CONFIGURATION REGISTERS

The system provides a number of configuration/status registers (CREG) to allow customization of the system. The CREGs are viewed and modified through the VDST host port. Some general notes about the CREG interface are provided below:

- When dealing with the CREGs all values are in **hexadecimal** (base 16) format.
- Only **lower case** hexadecimal values are understood by the system. For example, the input *abcd* will be classified as valid. The input *ABCD* will be rejected by the system.
- Care must be taken not to exceed the maximum valid CREG location when reading or writing CREG register location. **Do not attempt to access invalid CREG addresses.**
- Care must be taken when updating **CREGs 0x0018 ,0x0019, 0x0020, and/or 0x0021**. If invalid values are entered it is possible for the unit to become non-functional.

### 5.1 READING CREG VALUES

To read the current value at a CREG location:

1. At the VDST prompt, type the four-digit CREG address, then hit the ENTER key.
2. The VDST prints the register contents and then prints the prompt again.

For example, to view the contents CREG location 0x000C:

```
> 000c           <At the VDST prompt, type the CREG address, then hit the ENTER key.>
000C 0000       <The VDST prints the CREG address and then the current value>
>               <The VDST prints the prompt.>
```

### 5.2 WRITING CREG VALUES

To write a value to a CREG location:

1. At the VDST prompt, type the four-digit CREG address, then hit the ENTER key.
2. The VDST prints the register contents and then prints the prompt again.

For example, to write the contents CREG location 0x000C:

```
> 000c abcd      <At the VDST prompt, type address-space-value, then hit the ENTER key.>
000C abcd        <The VDST prints the CREG address and new value>
>               <The VDST prints the prompt.>
```



### 5.3 CONFIGURATION REGISTER SET SUMMARY

| Table 11. Configuration Register (CREG) Set Summary |   |             |               |
|---|---|-------------|---------------|
| Address Offset                                      | Register Name   | Access Type | Default State |
| 0x0000  | Reserved  | N/A         | N/A           |
| 0x0001  | Reserved  | N/A         | N/A           |
| 0x0002  | Mixer LINE_OUT Control (LINE_IN Volume)               | R/W         | 0x0000        |
| 0x0003  | Mixer LINE_OUT Control (MIC_IN Volume)                | R/W         | 0x0000        |
| 0x0004  | Mixer LINE_OUT Control (DEC_OUT Volume)               | R/W         | 0x7FFF        |
| 0x0005  | Mixer LINE_OUT Control (PCM_IN Volume)                | R/W         | 0x7FFF        |
| 0x0006  | Mixer PHONE_OUT Control (LINE_IN Volume)              | R/W         | 0x0000        |
| 0x0007  | Mixer PHONE_OUT Control (MIC_IN Volume)               | R/W         | 0x0000        |
| 0x0008  | Mixer PHONE_OUT Control (DEC_OUT Volume)              | R/W         | 0x7FFF        |
| 0x0009  | Mixer PHONE_OUT Control (PCM_IN Volume)               | R/W         | 0x7FFF        |
| 0x000A  | Mixer ENC_IN Control (LINE_IN Volume)                 | R/W         | 0x0000        |
| 0x000B  | Mixer ENC_IN Control (MIC_IN Volume)                  | R/W         | 0x0000        |
| 0x000C  | Mixer ENC_IN Control (DEC_OUT Volume)                 | R/W         | 0x0000        |
| 0x000D  | Mixer ENC_IN Control (PCM_IN Volume)                  | R/W         | 0x7FFF        |
| 0x000E  | Mixer PCM_OUT Control (LINE IN Volume)                | R/W         | 0x0000        |
| 0x000F  | Mixer PCM_OUT Control (MIC_IN Volume)                 | R/W         | 0x0000        |
| 0x0010  | Mixer PCM_OUT Control (DEC_OUT Volume)                | R/W         | 0x7FFF        |
| 0x0011  | Mixer PCM_OUT Control (PCM_IN Volume)                 | R/W         | 0x0000        |
| 0x0012  | CREG Save (0xAB10 = save to flash)                    | WO          | N/A           |
| 0x0013  | CREG Restore (0x01BA = load from flash)               | WO          | N/A           |
| 0x0014  | CREG Factory Default (0x1092 = load factory defaults) | WO          | N/A           |
| 0x0015  | Truncation Type (0 = 8 kfps, 1 = 6.667 kfps)          | R/W         | 0x0000        |
| 0x0016  | Truncation State (0 = NORMAL, 1 = TRUNCATED)          | RO          | 0x0000        |
| 0x0017  | PCM Clock Mode (0 = EXTERNAL, 1 = INTERNAL)           | R/W         | 0x0000        |
| 0x0018  | PCM Clock Rate Divider A (OPMODES 1 and 2)            | R/W         | 0x0008        |
| 0x0019  | PCM Frame Rate Divider A (OPMODES 1 and 2)            | R/W         | 0x01FF        |
| 0x001A  | Reserved  | N/A         | 0x0000        |
| 0x001B  | Reserved  | N/A         | 0x0000        |



**Table 11. Configuration Register (CREG) Set Summary**

| Address Offset | Register Name   | Access Type | Default State |
|----------------|---|-------------|---------------|
| 0x001C         | Error Flags   | R/W         | 0x0000        |
| 0x001D         | Reset Buffer Control (set = 0x8732 to reset/flush the buffers)<br>(same as RB bit in the Control/Status Byte) | WO          | N/A           |
| 0x001E         | Reserved  | N/A         | 0x0000        |
| 0x001F         | PCM Loop Back (0 = NONE, 1 = ALL, 2 = compressed voice ONLY)  | R/W         | 0x0000        |
| 0x0020         | PCM Clock Rate Divider B (OPMODE 3)   | R/W         | 0x0008        |
| 0x0021         | PCM Frame Rate Divider B (OPMODE 3)   | R/W         | 0x0265        |
| 0x0022         | Test Register 1 (must ALWAYS be 0x0000)   | R/W         | 0x0000        |
| 0x0023         | Test Register 2 (must ALWAYS be 0x0000)   | R/W         | 0x0000        |
| 0x0024         | Test Register 3 (must ALWAYS be 0x0000)   | R/W         | 0x0000        |
| 0x0025         | Host Port Capture (0 = enabled)   | R/W         | 0x0001        |
| 0x0026         | Host Port Playback (0 = enabled)  | R/W         | 0x0001        |
| 0x0027 +       | Reserved  | N/A         | N/A           |



## 5.4 CREG DETAILED DESCRIPTIONS

### 5.4.1 CREG Mixer Controls (0x0002 – 0x0011)

There are 4 audio sources and 4 audio destinations in the system. The 4 audio sources are LINE\_IN, MIC\_IN, PCM\_IN and DEC\_OUT (this output from the decoder is an input to the linear mixer). The 4 audio destinations are LINE\_OUT, PHONE\_OUT, PCM\_OUT and ENC\_IN (output from the linear mixer into the encoder).

Each audio destination has a set of 4 CREG registers that control the input value. The valid range of the input volumes are from 0x0000 (no audio) to 0x7FFF (maximum audio). See “4.2.2 Linear Voice Mixer” and Figure 3 for functional information.

For example, the LINE\_OUT signal mixer is controlled by CREG locations 0x0002 – 0x0005. To route LINE\_IN at half the volume to LINE\_OUT while disabling all other audio sources, enter the following sequence of commands at the host interface:

```
> 0002 3fff      <Set LINE_IN to half the maximum volume level>
0002 3FFF
> 0003 0000      <Set MIC_IN to zero volume level - disabled>
0003 0000
> 0004 0000      <Set DEC_OUT to zero volume level - disabled>
0004 0000
> 0005 0000      <Set PCM_IN to zero volume level - disabled>
0005 0000
```

### 5.4.2 CREG Save (0x0012)

The save command will save the current settings of the CREG registers to flash for later use. The values saved to flash will automatically be restored upon power up or by use of the CREG Restore (0x0013) register.

To save the current CREG setting to flash, write **ab10** to CREG **0012**.

### 5.4.3 CREG Restore (0x0013)

The restore command allows the CREG setting saved to flash to be retrieved.

To restore the CREG settings from flash, write **01ba** to CREG **0013**.

### 5.4.4 CREG Restore Factory Default (0x0014)

The restore factory default command will restore the current and saved CREGs to the factory default settings. The factory default settings are those listed as default values in Table 11.

To restore factory default settings, write **1092** to CREG **0014**.

### 5.4.5 CREG Truncation Type (0x0015)

The truncation type CREG determines the type of truncation (OPMODE = 2 or 3) when truncated mode is entered, e.g. when the TM bit is set. When CREG 0x0015 = 0001, the VDST will enter OPMODE = 2 when the TM bit is set. When CREG 0x0015=0000, the VDST will enter OPMODE = 3 when the TM bit set.

| Table 12. CREG Truncation Type (0x0015) |                             |                     |                        |
|---|-----------------------------|---------------------|------------------------|
| CREG Value                              | Operational Mode            | PCM Frame Rate (Hz) | Audio Sample Rate (Hz) |
| 0000                                    | Truncated Mode (OPMODE = 2) | 8000                | 6667                   |
| 0001                                    | Truncated Mode (OPMODE = 3) | 6667                | 6667                   |
|   | Normal Mode (OPMODE = 1)    | 8000                | 8000                   |

*Note: While CREG 0015 doesn't affect the normal mode, it has been included in the table for frame and sample rate comparison purposes.*

### 5.4.6 CREG Truncation State (0x0016)

The compression type CREG displays the current truncation state of the system. The truncation state of the system is determined by the TM bit on the PCM interface. The compression state is either NORMAL or TRUNCATED. This register is READ ONLY.

| Table 13. CREG Truncation State (0x0016) |  |
|--|--|
| CREG Value                               | Operational State                            |
| 0000                                     | Unit is functioning in <b>NORMAL</b> mode    |
| 0001                                     | Unit is functioning in <b>TRUNCATED</b> mode |

### 5.4.7 CREG PCM Timing Source Mode (0x0017)

The clock mode CREG determines the source of the clock and frame sync for the PCM interface. When internal timing is selected CREGs 0x0018 and 0x0019 may need to be modified to generate the desired frame sync and clock rates.

| Table 14. PCM Timing Source Mode (0x0017) |  |
|---|--|
| CREG Value                                | Operational State                                  |
| 0000                                      | Unit is functioning in <b>EXTERNAL</b> timing mode |
| 0001                                      | Unit is functioning in <b>INTERNAL</b> timing mode |



### 5.4.8 CREG PCM Clock Rate Divider A (0x0018)

The PCM clock rate divider, SCLKDIV, determines the clock rate for the PCM interface for operational modes 1 and 2 when the PCM interface is configured for INTERNAL timing mode. This register is ignored in external timing mode. An equation is used to calculate SCLKDIV parameter (used by the VDST DSP to generate the PCM clock rate):

$$SCLKDIV = \frac{DSP\_CLKOUT}{2 * (PCM\_CLK)} - 1$$

The *DSP\_CLKOUT* is fixed at 73.728 MHz. The *PCM\_CLK* is the desired clock rate for the PCM\_CLK signal on the PCM interface. See Appendix A for a list of pre-calculated values for 8000Hz frame rates.

*Note: A power cycle will be necessary for the values written to this register to take effect.*

*Note: It is recommended that CREG 0x0018 be written prior to CREG 0x0019.*

### 5.4.9 CREG PCM Frame Rate Divider A (0x0019)

The PCM frame rate divider, RFSDIV, determines the rate of the frame syncs generated for the PCM interface for operational modes 1 and 2 when the PCM interface is configured for INTERNAL timing mode. This register is ignored in external timing mode. An equation is used to calculate RFSDIV parameter (used by the VDST DSP to generate the PCM frame rate):

$$RFSDIV = \frac{PCM\_CLK}{PCM\_FS} - 1$$

The *PCM\_FS* is the desired frame rate for the PCM\_FS signal on the PCM interface. See Appendix A for a list of pre-calculated values for 8000 Hz frame rates.

*Note: A power cycle will be necessary for the values written to this register to take effect.*

*Note: It is recommended that CREG 0x0018 be written prior to CREG 0x0019.*





### 5.4.10 CREG Error Flags (0x001C)

The Error Flags register contains bit-mapped fields representing error conditions. If any of the bits are set, the ER bit is set on the PCM interface. The bits in this register are sticky, once set they need to be explicitly cleared even after the source of the error has been corrected. There are several ways to clear this register

- Directly writing a 0x0000 to the CREG
- Toggling the RB bit on the PCM interface (see “4.3.6 Control/Status Byte” for more information)
- Using the Reset Buffer CREG (0x001D).

It is possible for bits in the CREG to be set even after they have been explicitly cleared. This indicates that the source of the error has not been corrected.

| Table 15. Error Flag Register – Bit Assignments (0x001C) |    |    |    |    |    |   |   |   |   |   |      |      |      |      |   |
|--|----|----|----|----|----|---|---|---|---|---|------|------|------|------|---|
| 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4    | 3    | 2    | 1    | 0 |
| rsvd   |    |    |    |    |    |   |   |   |   |   | CVUR | CVOR | CVSE | rsvd |   |
| 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | X    | X    | X    | 0    | 0 |

**CVUE** Compressed Voice Packet Underrun Error. Set when an attempt is made to transmit a compressed voice packet over the PCM interface and there are no compressed voice packets available internally

**CVOE** Compressed Voice Packet Overrun Error. Set when the internal queue receiving compressed voice packets from the PCM interface has overflowed.

**CVSE** Compressed Voice Packet Sequence Error. Set when a sequence error is detected on the compressed voice packets received over the PCM interface

### 5.4.11 CREG Reset Buffer (0x001D)

The Reset Buffer CREG performs the same function as the RB bit. See “4.3.6 Control/Status Byte” for more information.

To reset the internal compressed voice buffers, write **8732** to CREG **001d**.

### 5.4.12 CREG PCM Loop Back (0x001F)

The PCM Loop Back CREG controls loopbacks the PCM interface.

| Table 16. PCM Timing Source Mode (0x0017) |  |
|---|--|
| CREG Value                                | Loopback State   |
| 0000                                      | <b>NORMAL:</b> No loop back.   |
| 0001                                      | <b>AGGREGATE LOOPBACK:</b> All data received on the PCM interface will be retransmitted on the PCM interface   |
| 0002                                      | <b>COMPRESSED VOICE LOOPBACK:</b> The received compressed voice packets are retransmitted on the PCM interface. The control/status byte and vocoder timing bits are not looped back. |



### 5.4.13 CREG PCM Clock Rate Divider B (0x0020)

The PCM clock rate divider, SCLKDIV, determines the clock rate for the PCM interface for operational mode 3 when the PCM interface is configured for INTERNAL timing mode. This register is ignored in external timing mode. See "5.4.8 CREG PCM Clock Rate Divider A (0x0018)" for the additional information.

See Appendix B for a list of pre-calculated values for 6667 Hz frame rates.

*Note: A power cycle will be necessary for the values written to this register to take effect.*

*Note: It is recommended that CREG 0x0020 be written prior to CREG 0x0021.*

### 5.4.14 CREG PCM Frame Rate Divider B (0x0021)

The PCM frame rate divider, RFSDIV, determines the rate of the frame syncs generated for the PCM interface for operational mode 3 when the PCM interface is configured for INTERNAL timing mode. This register is ignored in external timing mode. See "5.4.9 CREG PCM Frame Rate Divider A (0x0019)" for additional information.

See Appendix B for a list of pre-calculated values for 6667 Hz frame rates.

*Note: A power cycle will be necessary for the values written to this register to take effect.*

*Note: It is recommended that CREG 0x0020 be written prior to CREG 0x0021.*

### 5.4.15 CREG Test (0x0022 – 0x0024)

These registers MUST always be 0x0000. Incorrect VDST operation will result if any of these registers is non-zero.

### 5.4.16 CREG HOST Port Capture (0x0025)

This CREG location is used to enable HOST Port Capture. When the user sets the value to 0x0000, capture is enabled. When capture is disabled via the ESC-key, the VDST automatically sets the CREG to 0x0001.

| Table 17. HOST Port Capture (0x0025) |  |
|--------------------------------------|--|
| CREG Value                           | Operational State  |
| 0000                                 | HOST Port Capture is ENABLED.<br><i>Compressed voice messages are transmitted over the HOST port. PCM compressed voice transfer is disabled.</i> |
| 0001                                 | Normal Operation.<br><i>Compressed voice messages are transmitted over the PCM port. HOST Port Capture is disabled.</i>                          |



### 5.4.17 CREG HOST Port Playback (0x0026)

This CREG location is used to enable HOST Port Playback. When the user sets the value to 0x0000, playback is enabled. When capture is disabled via the ESC-key, the VDST automatically sets the CREG to 0x0001.

| Table 18. HOST Port Playback (0x0026) |   |
|---------------------------------------|---|
| CREG Value                            | Operational State   |
| 0000                                  | HOST Port Playback is ENABLED.<br><i>Compressed voice messages are received over the HOST port. PCM compressed voice reception is disabled.</i> |
| 0001                                  | Normal Operation.<br><i>Compressed voice messages are received over the PCM port. HOST Port Playback is disabled.</i>                           |



**APPENDIX A. PCM INTERNAL CLOCK SETTINGS (OPMODE 1/2 – 8000 FPS)**

| OPMODE1/2<br>CFG ID# | PCM<br>Clock Rate<br>(MHz) | PCM<br>Frame Rate<br>(kfps) | PCM<br>Bits/Frame | SCLKDIV A<br>[CREG 0018] | RFSDIV A<br>[CREG 0019] |
|----------------------|----------------------------|-----------------------------|-------------------|--------------------------|-------------------------|
| 1                    | 6.144000                   | 8.0104302                   | 767               | 5                        | 2FE                     |
| 2                    | 5.266286                   | 8.0034737                   | 658               | 6                        | 291                     |
| 3                    | 4.608000                   | 8.0000000                   | 576               | 7                        | 23F                     |
| <b>4 = Nominal</b>   | <b>4.096000</b>            | <b>8.0000000</b>            | <b>512</b>        | <b>8</b>                 | <b>1FF</b>              |
| 5                    | 3.686400                   | 8.0139130                   | 460               | 9                        | 1CB                     |
| 6                    | 3.351273                   | 8.0173989                   | 418               | A                        | 1A1                     |
| 7                    | 3.072000                   | 8.0208877                   | 383               | B                        | 17E                     |
| 8                    | 2.835692                   | 8.0104302                   | 354               | C                        | 161                     |
| 9                    | 2.633143                   | 8.0034737                   | 329               | D                        | 148                     |
| 10                   | 2.457600                   | 8.0052117                   | 307               | E                        | 132                     |
| 11                   | 2.304000                   | 8.0000000                   | 288               | F                        | 11F                     |
| 12                   | 2.168471                   | 8.0017365                   | 271               | 10                       | 10E                     |
| 13                   | 2.048000                   | 8.0000000                   | 256               | 11                       | FF                      |
| 14                   | 1.940211                   | 8.0173989                   | 242               | 12                       | F1                      |
| 15                   | 1.843200                   | 8.0139130                   | 230               | 13                       | E5                      |
| 16                   | 1.755429                   | 8.0156556                   | 219               | 14                       | DA                      |
| 17                   | 1.675636                   | 8.0173989                   | 209               | 15                       | D0                      |
| 18                   | 1.602783                   | 8.0139130                   | 200               | 16                       | C7                      |
| 19                   | 1.536000                   | 8.0418848                   | 191               | 17                       | BE                      |
| 20                   | 1.474560                   | 8.0139130                   | 184               | 18                       | B7                      |
| 21                   | 1.417846                   | 8.0104302                   | 177               | 19                       | B0                      |
| 22                   | 1.365333                   | 8.0313725                   | 170               | 1A                       | A9                      |
| 23                   | 1.316571                   | 8.0278746                   | 164               | 1B                       | A3                      |
| 24                   | 1.271172                   | 8.0453950                   | 158               | 1C                       | 9D                      |
| 25                   | 1.228800                   | 8.0313725                   | 153               | 1D                       | 98                      |
| 26                   | 1.189161                   | 8.0348736                   | 148               | 1E                       | 93                      |
| 27                   | 1.152000                   | 8.0000000                   | 144               | 1F                       | 8F                      |
| 28                   | 1.117091                   | 8.0366252                   | 139               | 20                       | 8A                      |
| 29                   | 1.084235                   | 8.0313725                   | 135               | 21                       | 86                      |
| 30                   | 1.053257                   | 8.0401309                   | 131               | 22                       | 82                      |
| 31                   | 1.024000                   | 8.0000000                   | 128               | 23                       | 7F                      |
| 32                   | 0.996324                   | 8.0348736                   | 124               | 24                       | 7B                      |
| 33                   | 0.970105                   | 8.0173989                   | 121               | 25                       | 78                      |
| 34                   | 0.945231                   | 8.0104302                   | 118               | 26                       | 75                      |
| 35                   | 0.921600                   | 8.0139130                   | 115               | 27                       | 72                      |
| 36                   | 0.899122                   | 8.0278746                   | 112               | 28                       | 6F                      |
| 37                   | 0.877714                   | 8.0524246                   | 109               | 29                       | 6C                      |
| 38                   | 0.857302                   | 8.0121713                   | 107               | 2A                       | 6A                      |
| 39                   | 0.837818                   | 8.0559441                   | 104               | 2B                       | 67                      |
| 40                   | 0.819200                   | 8.0313725                   | 102               | 2C                       | 65                      |
| 41                   | 0.801391                   | 8.0139130                   | 100               | 2D                       | 63                      |
| 42                   | 0.784340                   | 8.0034737                   | 98                | 2E                       | 61                      |
| 43                   | 0.768000                   | 8.0842105                   | 95                | 2F                       | 5E                      |



| <b>OPMODE1/2<br/>CFG ID#</b> | <b>PCM<br/>Clock Rate<br/>(MHz)</b> | <b>PCM<br/>Frame Rate<br/>(kfps)</b> | <b>PCM<br/>Bits/Frame</b> | <b>SCLKDIV A<br/>[CREG 0018]</b> | <b>RFSDIV A<br/>[CREG 0019]</b> |
|------------------------------|-------------------------------------|--------------------------------------|---------------------------|----------------------------------|---------------------------------|
| 44                           | 0.752327                            | 8.0034737                            | 94                        | 30                               | 5D                              |
| 45                           | 0.737280                            | 8.0139130                            | 92                        | 31                               | 5B                              |
| 46                           | 0.722824                            | 8.0313725                            | 90                        | 32                               | 59                              |
| 47                           | 0.708923                            | 8.0559441                            | 88                        | 33                               | 57                              |
| 48                           | 0.695547                            | 8.0877578                            | 86                        | 34                               | 55                              |
| 49                           | 0.682667                            | 8.0313725                            | 85                        | 35                               | 54                              |
| 50                           | 0.670255                            | 8.0753560                            | 83                        | 36                               | 52                              |
| 51                           | 0.658286                            | 8.0278746                            | 82                        | 37                               | 51                              |
| 52                           | 0.646737                            | 8.0842105                            | 80                        | 38                               | 4F                              |
| 53                           | 0.635586                            | 8.0453950                            | 79                        | 39                               | 4E                              |
| 54                           | 0.624814                            | 8.0104302                            | 78                        | 3A                               | 4D                              |
| 55                           | 0.614400                            | 8.0842105                            | 76                        | 3B                               | 4B                              |
| 56                           | 0.604328                            | 8.0577049                            | 75                        | 3C                               | 4A                              |
| 57                           | 0.594581                            | 8.0348736                            | 74                        | 3D                               | 49                              |
| 58                           | 0.585143                            | 8.0156556                            | 73                        | 3E                               | 48                              |
| 59                           | 0.576000                            | 8.0000000                            | 72                        | 3F                               | 47                              |

*Note: The VDST uses the ADSP-2188 processor SPORT0 port to drive the PCM interface.*



**APPENDIX B. PCM INTERNAL CLOCK SETTINGS (OPMODE 3 – 6667 FPS)**

| OPMODE 3<br>CFG ID# | PCM<br>Clock Rate<br>(MHz) | PCM<br>Frame Rate<br>(kfps) | PCM<br>Bits/Frame | SCLKDIV B<br>[CREG 0020] | RFSDIV B<br>[CREG 0021] |
|---------------------|----------------------------|-----------------------------|-------------------|--------------------------|-------------------------|
| 1                   | 6.144000                   | 6.6710098                   | 921               | 5                        | 398                     |
| 2                   | 5.266286                   | 6.6746334                   | 789               | 6                        | 314                     |
| 3                   | 4.608000                   | 6.6685962                   | 691               | 7                        | 2B2                     |
| <b>4 = Nominal</b>  | <b>4.096000</b>            | <b>6.6710098</b>            | <b>614</b>        | <b>8</b>                 | <b>265</b>              |
| 5                   | 3.686400                   | 6.6782609                   | 552               | 9                        | 227                     |
| 6                   | 3.351273                   | 6.6758421                   | 502               | A                        | 1F5                     |
| 7                   | 3.072000                   | 6.6782609                   | 460               | B                        | 1CB                     |
| 8                   | 2.835692                   | 6.6722172                   | 425               | C                        | 1A8                     |
| 9                   | 2.633143                   | 6.6831037                   | 394               | D                        | 189                     |
| 10                  | 2.457600                   | 6.6782609                   | 368               | E                        | 16F                     |
| 11                  | 2.304000                   | 6.6782609                   | 345               | F                        | 158                     |
| 12                  | 2.168471                   | 6.6722172                   | 325               | 10                       | 144                     |
| 13                  | 2.048000                   | 6.6710098                   | 307               | 11                       | 132                     |
| 14                  | 1.940211                   | 6.6673901                   | 291               | 12                       | 122                     |
| 15                  | 1.843200                   | 6.6782609                   | 276               | 13                       | 113                     |
| 16                  | 1.755429                   | 6.6746334                   | 263               | 14                       | 106                     |
| 17                  | 1.675636                   | 6.6758421                   | 251               | 15                       | FA                      |
| 18                  | 1.602783                   | 6.6782609                   | 240               | 16                       | EF                      |
| 19                  | 1.536000                   | 6.6782609                   | 230               | 17                       | E5                      |
| 20                  | 1.474560                   | 6.6722172                   | 221               | 18                       | DC                      |
| 21                  | 1.417846                   | 6.6879536                   | 212               | 19                       | D3                      |
| 22                  | 1.365333                   | 6.6928105                   | 204               | 1A                       | CB                      |
| 23                  | 1.316571                   | 6.6831037                   | 197               | 1B                       | C4                      |
| 24                  | 1.271172                   | 6.6903811                   | 190               | 1C                       | BD                      |
| 25                  | 1.228800                   | 6.6782609                   | 184               | 1D                       | B7                      |
| 26                  | 1.189161                   | 6.6806814                   | 178               | 1E                       | B1                      |
| 27                  | 1.152000                   | 6.6976744                   | 172               | 1F                       | AB                      |
| 28                  | 1.117091                   | 6.6891671                   | 167               | 20                       | A6                      |
| 29                  | 1.084235                   | 6.6928105                   | 162               | 21                       | A1                      |
| 30                  | 1.053257                   | 6.7086442                   | 157               | 22                       | 9C                      |
| 31                  | 1.024000                   | 6.6928105                   | 153               | 23                       | 98                      |
| 32                  | 0.996324                   | 6.6867404                   | 149               | 24                       | 94                      |
| 33                  | 0.970105                   | 6.6903811                   | 145               | 25                       | 90                      |
| 34                  | 0.945231                   | 6.7037643                   | 141               | 26                       | 8C                      |
| 35                  | 0.921600                   | 6.6782609                   | 138               | 27                       | 89                      |
| 36                  | 0.899122                   | 6.7098653                   | 134               | 28                       | 85                      |
| 37                  | 0.877714                   | 6.7001091                   | 131               | 29                       | 82                      |
| 38                  | 0.857302                   | 6.6976744                   | 128               | 2A                       | 7F                      |
| 39                  | 0.837818                   | 6.7025455                   | 125               | 2B                       | 7C                      |
| 40                  | 0.819200                   | 6.7147541                   | 122               | 2C                       | 79                      |
| 41                  | 0.801391                   | 6.6782609                   | 120               | 2D                       | 77                      |
| 42                  | 0.784340                   | 6.7037643                   | 117               | 2E                       | 74                      |
| 43                  | 0.768000                   | 6.6782609                   | 115               | 2F                       | 72                      |



| <b>OPMODE 3<br/>CFG ID#</b> | <b>PCM<br/>Clock Rate<br/>(MHz)</b> | <b>PCM<br/>Frame Rate<br/>(kfps)</b> | <b>PCM<br/>Bits/Frame</b> | <b>SCLKDIV B<br/>[CREG 0020]</b> | <b>RFSDIV B<br/>[CREG 0021]</b> |
|-----------------------------|-------------------------------------|--------------------------------------|---------------------------|----------------------------------|---------------------------------|
| 44                          | 0.752327                            | 6.7172012                            | 112                       | 30                               | 6F                              |
| 45                          | 0.737280                            | 6.7025455                            | 110                       | 31                               | 6D                              |
| 46                          | 0.722824                            | 6.6928105                            | 108                       | 32                               | 6B                              |
| 47                          | 0.708923                            | 6.6879536                            | 106                       | 33                               | 69                              |
| 48                          | 0.695547                            | 6.6879536                            | 104                       | 34                               | 67                              |
| 49                          | 0.682667                            | 6.6928105                            | 102                       | 35                               | 65                              |
| 50                          | 0.670255                            | 6.7025455                            | 100                       | 36                               | 63                              |
| 51                          | 0.658286                            | 6.7172012                            | 98                        | 37                               | 61                              |
| 52                          | 0.646737                            | 6.6673901                            | 97                        | 38                               | 60                              |
| 53                          | 0.635586                            | 6.6903811                            | 95                        | 39                               | 5E                              |
| 54                          | 0.624814                            | 6.7184254                            | 93                        | 3A                               | 5C                              |
| 55                          | 0.614400                            | 6.6782609                            | 92                        | 3B                               | 5B                              |
| 56                          | 0.604328                            | 6.7147541                            | 90                        | 3C                               | 59                              |
| 57                          | 0.594581                            | 6.6806814                            | 89                        | 3D                               | 58                              |
| 58                          | 0.585143                            | 6.7257800                            | 87                        | 3E                               | 56                              |
| 59                          | 0.576000                            | 6.6976744                            | 86                        | 3F                               | 55                              |

*Note: The VDST uses the ADSP-2188 processor SPORT0 port to drive the PCM interface.*

